

We Claim:

1. A system for detecting a pattern in a data stream comprising:
 - a FIFO for receiving an N-bit wide data stream and a corresponding first clock signal at a first rate, and outputting the data stream as a W times N-bit wide data stream and a corresponding second clock signal at a second rate, where W is an integer natural number and the second rate equals the first rate divided by W;
 - a bus splitter for splitting the W times N-bit wide data stream into W data streams of width N;
 - a plurality (W) of RAMs, each RAM for storing data obtained by processing the pattern and for receiving a respective one of the data streams of width N as an address and the second clock signal as a clock, and each RAM being operable to output a portion of the data on an M-bit wide output bus in accordance with a value of the address; and
 - a processor for receiving the portions of data on each M-bit wide output bus as data and the second clock signal as a clock, and being operable to determine whether the pattern is in the data stream in dependence upon the received portions of data and the received clock, and for outputting a pattern match signal indicating detection of the pattern in the data stream.
2. The system as defined in claim 1 wherein the processor comprises shift/and combinatory logic and a register.
3. The system as defined in claim 1 having channelization functionality including an input channel register and a channel state RAM running C times slower than the first rate.
4. The system as defined in claim 3 wherein the processor includes means to update the channel state RAM in response to a state change.

5. A system for detecting a pattern in a data stream comprising:
 - an input stream register for receiving the data stream and a corresponding first clock signal at a first rate, and outputting the data stream and a corresponding second clock signal at a second rate;
 - a pattern RAM for storing a pattern to be detected;
 - a processor for receiving the data and the second clock signal as a clock, and being operable to determine whether the pattern is in the data stream in dependence upon the received data and the received clock, and for outputting a pattern match signal indicating detection of the pattern in the data stream
 - a channel state RAM for storing the state of the processor and running C times slower the data rate
 - a multiplexer that redirects either the contents of the processor's register or the contents of the channel state RAM to the processor; and
 - a channel register to switch the processor in dependence on the received data.
6. The system as defined in claim 5 wherein said input stream register is a FIFO for receiving an N-bit wide signal and having bus splitting means to divide said stream into W signals, each of said W signal provided to separate pattern RAMs.
7. The system as described in claim 1 wherein the data stream is of a known length.
8. The system as described in claim 5 wherein the data stream is of a known length.

9. The system as described in claim 1 adapted to detect a pattern of arbitrary length wherein the length is less than a set value.
10. The system as described in claim 5 adapted to detect a pattern of arbitrary length wherein the length is less than a set value.
11. The system as described in claim 9 wherein multiple engines are chained to detect a pattern of any arbitrary length.
12. A processor for use in a pattern matching engine, the processor having combinatory logic means for receiving outputs from pattern matching RAMs;
a register and an And Gate for combining the outputs from respective logic means to output an indication of a matched pattern.
13. A method of detecting a pattern in a data stream comprising:
receiving, at a FIFO, an N-bit wide data stream and a corresponding first clock signal at a first rate, and outputting the data stream as a W times N-bit wide data stream and a corresponding second clock signal at a second rate, where W is an integer natural number and the second rate equals the first rate divided by W;
splitting the W times N-bit wide data stream into W data streams of width N;
providing a plurality (W) of RAMs, each RAM for storing data obtained by processing the pattern and for receiving a respective one of the data streams of width N as an address and the second clock signal as a clock, and each RAM being operable to output a portion of the data on an M-bit wide output bus in accordance with a value of the address; and
receiving the portions of data on each M-bit wide output bus as data and the second clock signal as a clock at a processor, the processor being operable to determine whether the pattern is in the data stream in dependence upon the

received portions of data and the received clock, and outputting a pattern match signal indicating detection of the pattern in the data stream.

14. The method as defined in claim 13 further comprising:

providing means for adding channelization functionality in order to separate the input stream into channels for pattern matching.

15. A method of detecting a pattern in a data stream comprising:

receiving the data stream and a corresponding first clock signal at a first rate at an input stream register and outputting the data stream and a corresponding second clock signal at a second rate;

storing a pattern to be detected at a pattern RAM;

receiving the data and the second clock signal as a clock at a processor, the processor being operable to determine whether the pattern is in the data stream in dependence upon the received data and the received clock, and outputting a pattern match signal indicating detection of the pattern in the data stream;

providing a channel state RAM for storing the state of the processor and running C times slower the data rate

redirecting either the contents of the processor's register or the contents of the channel state RAM to the processor; and

switching the processor in dependence on the received data.

16. The method as defined in claim 15 wherein multiple pattern matching RAMs are provided to provide scalability.